

WHAT IS CLAIMED IS:

1.    An apparatus for providing an input output from an  
5    integrated circuit, the apparatus comprising:

        an upper pair of P-channel Metal Oxide Semiconductor  
(PMOS) devices coupled between a power supply ( $V_{DD0}$ ) and an I/O  
pad;

        a lower pair of N-channel MOS devices (NMOS), coupled  
10    between the I/O pad and a ground potential;

        a first bias circuit providing a first bias voltage to  
the first upper PMOS device when the I/O pad is in an output  
mode and  $V_{DD0}$  voltage otherwise;

        a second bias circuit providing a second bias voltage to  
15    the second lower NMOS device when the I/O pad is in an output  
mode and a ground voltage otherwise;

        a third bias circuit providing a first fixed voltage to  
the second upper PMOS device when  $V_{PAD}$  is less than the  $V_{DD0}$   
voltage and a voltage equal to  $V_{PAD}$  otherwise; and

20    a fourth bias circuit providing a second fixed voltage  
when  $V_{PAD}$  is less than a pre-determined value and a voltage  
higher than the second fixed voltage otherwise.

2.    The apparatus of claim 1 further comprising a well  
25    biasing circuit which provides a well bias to the upper pair  
of PMOS devices.

3.    The apparatus of claim 2 wherein the well biasing  
circuit provides a bias voltage of  $V_{DD0}$  if a voltage on the I/O  
30    pad is less than  $V_{DD0}$  and provides the voltage on the I/O pad  
as the bias voltage otherwise.

4.    The apparatus of claim 1 further comprising:  
        a NMOS device having a drain coupled to  $V_{PAD}$ ;  
35    the NMOS device having a source coupled to core circuitry; and

1      **50717/PAN/B600** - BP1708CON

having the gate coupled to the fourth bias voltage.

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